

1 Description

2 Switching device for bidirectionally equalizing charge between
3 energy accumulators and corresponding methods

4

5 The invention relates to a switching device for bidirectionally
6 equalizing charge between energy accumulators, especially
7 between capacitive energy accumulators in a motor vehicle
8 electrical system provided with an integrated starter-
9 generator. The invention further relates to a motor vehicle
10 electrical system with such a switching device, a method for
11 operating the switching device as well as to the use of a
12 switching controller in a switch.

13

14 Previously motor vehicles used a vehicle electrical system with
15 a system voltage of 14 V, which enables a charge voltage for
16 the accumulator of 12 V to be implemented. The output power
17 here is usefully limited for technical reasons to a maximum of
18 2 KW, since otherwise currents which are too great would flow
19 in the electrical system. With a 14 V vehicle electrical system
20 voltage, although the starter-generator can start the internal
21 combustion engine and supply the electrical loads during the
22 journey, power of more than 2 KW is required for further
23 functions such as boost (acceleration) or recuperation
24 (regenerative braking). This power can only be achieved with a
25 higher vehicle electrical system voltage and thereby with a

1 higher electrical power in the motor vehicle. Thus future
2 vehicle electrical systems are to be equipped with a higher
3 vehicle electrical system voltage of for example 42 V (this
4 corresponds to a charge voltage of the accumulator of 36 V), so
5 that around three times the power is available with the same
6 current.

7

8 Different forms of a generator mounted directly on the
9 crankshaft have been developed as primary energy sources, which
10 - in a reversal of its principle of operation - can also be
11 used as and electric motor and thereby as a starter for
12 supporting the internal combustion engine. This generator is
13 referred to as an integrated starter-generator (ISG). When
14 operated in generating mode, the ISG allows electrical power to
15 be generated and when operated in motor mode it enables
16 mechanical drive power to be generated. In addition to the
17 significantly increased power compared to known 2 KW generators
18 (around 6 KW for an ISG) and in addition to its original
19 function such as engine starting and electrical system supply,
20 an ISG provides the following additional functions:

21

22 - Boost (acceleration): Torque support for the internal
23 combustion engine during the acceleration phase of the
24 motor vehicle. The ISG has a maximum torque of around 200
25 Nm, which approximately corresponds to the torque of an

1 internal combustion engine. During the boost process,
2 currents of up to 270 A are needed for around 10 - 15
3 seconds to provide this torque.

- 4
- 5 - Recuperation (regenerative braking): The ISG dissipates
6 kinetic energy during vehicle braking by power generation.
7 In this case currents of up to 270 A are created for up to
8 30 seconds which are again stored in the form of electrical
9 energy.
- 10 - Stop and go (engine shutdown when the vehicle is stopped,
11 fast start of the internal combustion engine on restart).

12

13 Model computations and measurements on test vehicles have
14 produced fuel savings of over 20% when the ISG is used in city
15 traffic or with a corresponding driving cycle when utilizing
16 the above new functions. If the ISG is essentially to be used
17 for the fuel saving function, the motor vehicle electrical
18 system must be in a position to provided significant power over
19 the short term or store it again. With peak currents of 800 A
20 this involves power in the range of 10 KW. Conventional 14 V
21 starter batteries (accumulators), as well as future 42 V
22 starter batteries are however not able to provide such high
23 peak currents or to accept them again. When other accumulator
24 types are used, for example nickel-cadmium batteries, nickel-
25 metal-hydride batteries or lithium-ion batteries, such high

1 peak currents can under some circumstances be accommodated.
2 However such battery types do not meet or only inadequately
3 meet other requirements for the electrical system, such as a
4 high cycle strength for example. In particular current battery
5 types must be designed to handle 300,000 to 500,000 charge and
6 discharge cycles, as are typical for the boost and recuperation
7 function of the ISG. Such high changes of cycle cannot be
8 handled by current known battery types (accumulators) for motor
9 vehicle applications.

10

11 Only a few energy accumulators are in any position to provide
12 the required high cycle number or the high energy throughput -
13 for 200.000 boost processes a total of appr. 12.6 MWh of energy
14 or appr. 180,000 Ah are needed. Only Double-Layer Capacitors
15 (DLC) have proved for a variety of reasons to be suitable
16 energy accumulators for the fuel saving functions described
17 above. Double-layer capacitors are able to store the high
18 energy converted on boost and recuperation and output it again.
19 The currents occurring in such cases also do not present any
20 problems for double-layer capacitor functions. Because of their
21 very high efficiency there is also very little self-heating and
22 thereby a long life expectancy. The limited energy accumulator
23 capacity of a double-layer capacitor however makes an
24 additional accumulator, for example a simple lead-acid
25 accumulator, necessary. This accumulator is not subject to a

1 cyclic load from the frequent cycle changes so that a
2 relatively long lifetime is to be expected by today's
3 standards.

4

5 A disadvantage in the use of double-layer capacitors as energy
6 accumulators however lies in the fact that an exchange of
7 energy at the capacitor is necessarily also associated with a
8 voltage change. To move 75% of the charge, the capacitor
9 voltage must be varied by 50%. For a 42 V vehicle electrical
10 system this would for example mean a voltage variation of 21 V
11 to 42 V in the fully charged state. However such a voltage
12 variation is not acceptable for a motor vehicle electrical
13 system, since this system requires a voltage which is as stable
14 as possible.

15

16 02/066192 A1 describes a motor vehicle electrical system in
17 which the ISG is dynamically connected to the 42 V vehicle
18 electrical system and the double-layer capacitor by means of a
19 number of power switches. In the normal driving mode these
20 connecting switches embodied as power switches connect the ISG
21 and 42 V vehicle electrical system to each other. Only for the
22 duration of the fuel saving functions, which can typically last
23 a maximum of 10 seconds, are the ISG and the double-layer
24 capacitor connected to each other. In this way it can be
25 guaranteed that the 42 V vehicle electrical system and the

1 double-layer capacitor are always physically separated, so that
2 different voltage potentials have no role to play here either.

3

4 The main emphasis in implementing the connecting switch between
5 ISG and 42 V vehicle electrical system or double-layer
6 capacitor respectively is primarily on the controlled switch-on
7 of the connecting switches, since two very low-resistance
8 energy sources are connected to each other in each case with a
9 smoothing capacitor at the ISG and the 42 V battery or with the
10 smoothing capacitor and the double-layer capacitor. To
11 implement a fuel saving function which is a great as possible,
12 the connecting switches are controlled so that a required
13 charge equalization can be undertaken in a very well controlled
14 manner where possible.

15

16 The vehicle electrical system described in 02/066293 A1 is
17 designed for the optimum fuel saving function. With many
18 applications the vehicle electrical system, in addition to its
19 fuel saving function - especially electrical boost support -
20 must additionally meet other requirements. Thus in many
21 applications, especially for high-priced motor vehicles,
22 driving convenience also has an especially great role to play.
23 The need thus arises to find a synthesis between the two
24 requirements of the greatest possible driving comfort and the
25 highest possible fuel savings.

1
2 This is best achieved by the energy recovered during
3 regenerative braking and stored in the double-layer capacitor
4 being fed directly to the 42 V vehicle electrical system where
5 necessary. However the double-layer capacitor is no longer
6 separated from the 42 V vehicle electrical system, but would -
7 even for only short time - be directly connected to it. This is
8 to be avoided however. In order on the one hand to provide a
9 physical separation between double layer capacitor and 42 V
10 vehicle electrical system and on the other hand to meet the
11 requirement of directly feeding the stored energy of the double
12 layer capacitor where necessary back into the 42 V vehicle
13 electrical system, an expansion of the functionality of at
14 least one of the connection switches between ISG and 42 V
15 vehicle electrical system or double-layer capacitor
16 respectively is required.

17
18 The object of the present invention is thus to specify a
19 switching device which is as simple as possible which allows
20 such feeding back of the energy recovered by the double-layer
21 capacitor into the vehicle electrical system and which still
22 allows a physical separation between double-layer capacitor and
23 vehicle electrical system.

24
25 In accordance with the invention this object is achieved by a

1 switching device with the features of claim 1. Furthermore a
2 motor vehicle electrical system with the features of claim 20,
3 a method with the features of claim 26 and an application with
4 the features of claim 37 are provided.

5

6 The idea underlying the present invention consists of using at
7 least one transferred gate which exhibits an expanded
8 functionality as a connection switch. Such a transfer gate is
9 arranged between the vehicle electrical system and the double-
10 layer capacitor or and also between one of these elements and
11 the starter-generator. The transfer gate provides an especially
12 efficient solution for separating the vehicle electrical system
13 and the double-layer capacitor and for connecting these
14 elements to the starter-generator. As a result of the high
15 currents the transfer gate consists of a parallel circuit of
16 two controllable power switches connected in series in each
17 case. Their source connections are connected to each other each
18 case. The important factor here is that at least one branch of
19 the transistors switched in parallel, that is one of the series
20 circuits, is embodied as a switching controller which can be
21 operated bidirectionally. Advantageously this switching
22 controller is embodied as a downward controller. The expanded
23 functionality of the transfer gate is thus produced by
24 providing an additional switching controller of which the load
25 path is arranged in parallel to the load paths of the transfer

1 gates, as well as an activation circuit for activation of the
2 transfer gate and of the switching controller.

3

4 The power switches of the inventive switching device are
5 advantageously embodied as power MOSFETs, JFETs, thyristors,
6 IGBTs or such like would also be conceivable.

7

8 The inventive transfer gate now allows an equalization of the
9 charge between the intermediate circuit capacitor and the
10 double-layer capacitor or between the intérmediate circuit
11 capacitor and the battery which is advantageously equipped with
12 an optimum efficiency. The inventive transfer gate thus allows
13 typical efficiencies of 85% to be implemented. By contrast,
14 with previous applications, for example conventional transfer
15 gates without switching controllers or power switches,
16 efficiencies of up to only 50% can be implemented, since around
17 50% of the charge difference was converted into heat in the
18 connection switches or in the power resistor respectively.

19

20 Using the inventive switching device with expanded transfer
21 gates also allows discharging of the double-layer capacitor
22 down to the voltage level of the 42 V vehicle power system.
23 This is also desirable in order to enable the energy recovered
24 on regenerative braking to be fed back into the vehicle
25 electrical system for an internal combustion engine when

1 idling.

2

3 Advantageously a recharging of the double-layer capacitor up to
4 the voltage level of the vehicle electrical system is possible.
5 This is also desirable in order to recharge for example a
6 double-layer capacitor which has become discharged after
7 several weeks during which the vehicle has been stopped and to
8 start the vehicle using the charged-up double-layer capacitor.

9

10 The inventive solution is also economical to the extent that
11 its allows a current equalization for currents of around 30 A
12 to appr. 100 A and with the transfer gate activated allows
13 switch currents of up to appr. 1,000 A. The power transistors
14 of the switching controller or of the transfer gate in this
15 case carry a partial current, so that a multiple use of these
16 transistors is advantageously implemented here.

17

18 Preferably the starter-generator is connected to rotate in a
19 fixed manner with the drive train, but it can also be belt
20 driven.

21

22 Advantageous embodiments and developments of the invention are
23 produced from the further subclaims as well as from the
24 description which refers to the drawings.

25 The invention is described in more detail below on the basis of

1 the exemplary embodiments specified in the schematic figures of
2 the drawing. The drawing shows:

3

4 Figure 1 a basic circuit diagram of an inventive motor vehicle
5 electrical system, in which the function of a
6 connecting switch is replaced by an inventive
7 switching device with expanded transfer gate;

8

9 Figure 2 with reference to of a circuit diagram, a simplified
10 exemplary embodiment of an inventive transfer gate
11 expanded by a switching controller for an inventive
12 switching device;

13

14 Figure 3 a block diagram of an inventive switching device with
15 a transfer gate and a switching controller from
16 Figure 2 as well as an activation circuit for
17 activation of the switching controller and further
18 functional units;

19

20 Figure 4 a more detailed circuit diagram of a transfer gate of
21 an inventive switching device with charge pump and
22 activation circuit;

23

24 Figure 5 a more detailed circuit diagram of a switching
25 controller of the inventive switching device;

1

2 Figure 6 the connections of a power MOSFET embodied as a

3 measurement transistor for a switching controller

4 from Figure 5;

5

6 Figure 7 a circuit diagram for showing the auxiliary power

7 source for supplying the gate control circuit of the

8 switching controller from Figure 5;

9

10 Figure 8 a circuit diagram of a gate control circuit for

11 control of the switching controller from Figure 5;

12

13 Figure 9 a circuit diagram of the voltage sensing device of

14 the inventive switching device with polarity

15 detection and absolute value generation;

16

17 Figure 10 a circuit diagram for the sequence control circuit of

18 the inventive switching device.

19

20 In all Figures of the drawing the same elements and signals or

21 those with the same function - unless otherwise specified -

22 have been provided with the same reference symbols.

23

24 Figure 1 shows a basic circuit diagram of an inventive motor

25 vehicle electrical system, in which the function of a

1 connection switch is replaced by an inventive switching device
2 with expanded transfer gate.

3

4 Reference symbol 1 in Figure 1 designates the motor vehicle
5 electrical system. The motor vehicle electrical system 1
6 consists of an integrated starter-generator 2 - referred to
7 below by the abbreviation ISG - which is coupled mechanically
8 to an internal combustion engine 3. The ISG is an asynchronous
9 machine which is connected via a bidirectionally operable AC/DC
10 converter 4 and an intermediate circuit capacitor 5 to a power
11 supply. The power supply consists on the one hand of a double-
12 layer capacitor 6 - designated below by the abbreviation DLC
13 capacitor - and on the other hand of an accumulator 7, at which
14 a voltage of 36/42 V is present (rated voltage 36 V, in the
15 fully charged state 42 V). From this accumulator 7 loads can be
16 fed directly via an output 8. The said voltage of 36/42 V is
17 present at output 8. The DLC capacitor 6 is connected via a
18 first switch 9 to the ISG 2, the accumulator 7 is connected via
19 a second switch 10 to the ISG. With suitable activation of
20 these controllable switches 9, 10, energy stored in the DLC
21 capacitor 6 can be fed into the accumulator 7.

22

23 Under normal driving conditions the ISG 2 of the internal
24 combustion engine 3 will be driven and thus operates in
25 generator mode. Under such conditions it charges the energy

1 accumulator with energy, which can occur under normal driving
2 conditions at low power. In the recuperation mode this charging
3 up is undertaken at increased power, corresponding the maximum
4 power output of the ISG 2. For a 6-KW ISG 2 this means a
5 maximum charge current of over 250 A.

6

7 This basic layout of such a motor vehicle electrical system
8 with ISG and double-layer capacitor is already described in
9 02/066192 A1 cited at the start, which as regards the general
10 layout and functioning of a motor vehicle electrical system,
11 ISGs, double layer capacitors and the switch, is fully included
12 as regards contents in the present patent application.

13

14 In accordance with the invention at least one of the controlled
15 switches 9, 10 is now embodied as an inventive switching device
16 with a transfer gate, switching controller and expanded
17 functionality. The inventive switching device thus initially
18 has the function of a controlled switch. In addition - as will
19 be explained below in greater detail - the switching process is
20 controlled by the switching device, especially as regards the
21 voltage dropping over the switch, so that the switching-related
22 losses remain low or a conventional energy flow from the
23 double-layer capacitor 6 to the accumulator 7 and vice-versa is
24 possible.

25

1 Figure 2 shows a circuit diagram of a simplified exemplary
2 embodiment of an inventive transfer gate expanded by a
3 switching controller for an inventive switching device.

4

5 The inventive switching device identified by reference symbol
6 20 contains a switching controller 21 as well as a transfer
7 gate arranged in parallel to this. This parallel circuit
8 comprising switching controller 21 and transfer gate 29 is
9 arranged between a first terminal 22 and a second terminal 23.
10 These two terminals 22, 23, depending on the direction in which
11 a current is to be switched, can be operated both as an input
12 terminal and as an output terminal. In the present exemplary
13 embodiment terminal 22 is operated as input terminal and
14 terminal 23 as output terminal.

15

16 During operation of the inventive switching device 20 a first
17 potential V1 is present as the input terminal 22 and a second
18 potential V2 at the output terminal 23, so that the
19 differential voltage $V_{diff} = V2 - V1$ is present between the
20 terminals 22, 23 and thereby across the switching device 20.

21

22 The inventive transfer gate 20 consists of a parallel circuit
23 of two power MOSFETs T1 - T6 connected to each other in series.
24 Such a transistor pair defines a load path, so that the
25 transfer gate 29 is constructed from the parallel connection of

1 a number of such load paths. The two power MOSFETs T1 - T6 of a
2 relevant load path are short circuited to each other via their
3 gate terminals and their source terminals. The respective drain
4 terminals of the power MOSFETs T1 - T6 are connected either to
5 the input terminal 22 or the output terminal 23. The series
6 circuit of two power MOSFETs T1 - T6 of a relevant load path is
7 produced by the corresponding series-connected links of these
8 transistors T1 - T6. The reason for a series circuit is that
9 the leading sign of the voltage at the opened power MOSFET is
10 not defined and the substrate diode of one of these power
11 MOSFETs T1 - T6 respectively is polarized in the on-state
12 direction. Depending on application and requirement the three
13 parallel-switched load paths of the transfer gate 29 at the
14 terminals A - D can be expanded by further branches with power
15 MOSFET pairs.

16

17 The switching controller 21 consists of two power transistors
18 27, 28, which are activated via their gate terminals E, F. The
19 precise activation of these power MOSFETs 27, 28 will be
20 described in greater detail below. The controlled links of the
21 power MOSFETs 27, 28 are coupled to each other via a choke 24,
22 for example a coil or a such an inductive element. The source
23 terminals of the transistors 27, 28 are further connected in
24 each case via a free-wheeling diode 25, 26 to a reference
25 potential GND. The drain-side terminals of the transistors 27,

1 28 are connected to the terminals 22, 23.

2

3 Figure 3 shows a block diagram of an inventive switching device
4 with a transfer gate and a switching controller from Figure 2
5 as well as an activation circuit for activation of the
6 switching controller and transfer gate and further functional
7 units.

8

9 A central element of the inventive switching device 20 is a
10 control device 36 which serves to control or regulate the
11 function of the switching controller 21 and thus monitors its
12 switching processes. The control unit 36 can for example be
13 embodied as a program-controlled device, for example as a
14 microcontroller or microprocessor. Controlled by an external
15 "On/Off" signal the control unit 36 opens or closes the
16 connection between the terminals 22, 23. In response to this
17 "On/Off" signal, the control unit 36 delivers the signal
18 "Switch ON" to an external control unit (not shown) when the
19 required switching state of the switching controller 21 is
20 reached. It further creates a further "diagnosis" signal, which
21 is used to monitor the overall function of the switching
22 controller 21. This "diagnosis" signal is expandable up to the
23 point of detailed error analysis.

24

25 The switching controller 21 consists of a number of functional

1 groups which are mostly arranged symmetrically to the inductor
2 24. In this case the gate terminals of the power MOSFETs 27, 28
3 are connected to gate controllers 30, 31. For control of the
4 power MOSFETs 27, 28 these gate controllers 30, 31 are fed
5 control signals Ctrl1, Ctrl2 of the control unit 36. The gate
6 controller 30, 31 controls the power MOSFETs 27, 28 as a
7 function of signals Ctrl1, Ctrl2, so that one of these power
8 MOSFETs 27, 28 in each case is switched on or switched off by
9 the clock of the signals Ctrl1, Ctrl2.

10

11 The power MOSFETs 27, 28 are embodied as N-channel MOSFETs in
12 the present exemplary embodiment. A gate potential above the
13 drain potential and thereby above a potential of a signal V1,
14 V2 connected in via the terminals 22, 23 is thus needed to
15 switch on the transistors 27, 28. For these purposes an
16 auxiliary power source 32, 33 is provided for each of the power
17 MOSFETs 27, 28, which is connected to the relevant gate
18 controllers 30, 31 and which provides the relevant gate
19 potential for activation of the transistors 27, 28.

20

21 Furthermore current measurement devices 35, 36 are provided
22 which are connected to the substrate terminals and source
23 terminals of the power MOSFETs 27, 28 and which are designed to
24 measure a current in the load path of these power MOSFETs 27,
25 28. Using this as its starting point, the current sensing

1 device 35, 36 creates current sensing signals CS1, CS2 (CS =
2 Current Sense) which are fed to the control unit 36 and are
3 used for control and supervision of the functional sequence of
4 the switching controller 21.

5

6 Furthermore a voltage sensing device 37 is provided which is
7 connected to the drain terminals of the power MOSFETs 27, 28.
8 The voltage sensing device 37 records the potentials V1, V2 at
9 the terminals 22, 23 and thereby a differential voltage Vdiff
10 falling at the switching controller 21. In this case the
11 voltage sensing device 37 on the one hand detects the polarity
12 of this differential voltage Vdiff and creates the digital
13 signal Vdiff1 as a function of this. On the other hand the
14 voltage sensing device 37 records the absolute value of this
15 differential voltage Vdiff and outputs the amount of this
16 differential voltage Vdiff as a ground-related voltage value
17 Vdiff2. A reference voltage Vref is also required for the
18 function of the voltage sensing device 37. The signals Vdiff1,
19 Vdiff2 provided on the output side of the voltage sensing
20 device 37 are fed to the control unit 36 for control and
21 monitoring purposes.

22

23 The circuit arrangement in Figure 3 further shows a function
24 block 29 which contains the actual transfer gate. The transfer
25 gate 29 is arranged in parallel to the switching controller 21

1 and thus connected between the input 22 and the output 23. The
2 transfer gate 29 can be switched on or off using the control
3 signal TGon of the control unit 36 is.

4

5 The function of the inventive switching device 20 shown in
6 Figure 3 is briefly explained below.

7

8 It is first assumed that the switching device 20 is open,
9 meaning that the "On/Off" signal exhibits a low logical level.
10 Let a potential V1 at input 22 be greater than the potential V2
11 at output 23. The transistors 27, 28 as well as a charge pump
12 for activation of these transistors 27, 28 is switched off.
13 For the switch-on process of the switching device 20 the
14 control unit 36 now receives a control signal to close the
15 switching device for example, by setting the "On/Off" signal to
16 a high logical level.

17

18 1. Switch-on process:

19 In a first step the potential difference Vdiff between input 22
20 and output 23 is equalized by means of the switching controller
21 21, before the switching controller 21 is completely closed in
22 a second step.

23

24 2. Preparation:

25 Initially a voltage difference Vdiff2 and a voltage polarity

1 Vdiff1 (Vdiff2 > 0, Vdiff1 = HIGH) are measured by the voltage
2 sensing device 37 and evaluated in the control unit 36.

3

4 3. The following decisions are now taken in the control unit
5 36:

- 6 - The voltage difference Vdiff2 is greater than an upper
7 threshold value. This results in a charge equalization
8 being required by operating the switching controller.
- 9 - The voltage difference Vdiff1 has a positive polarity. This
10 results in transistor 27 being selected as switching
11 controller transistor and transistor 28, which is operated
12 here with reverse polarity, being switched on statically.
13 Furthermore the current sensing signal CS2 for is selected
14 for current sensing.
- 15 - The transfer gate 29 initially remains switched off.
16 If the control unit 36 was to determine that the voltage
17 difference Vdiff2 is smaller than a lower threshold value,
18 the process jumps directly at this point to Para. 5 below.

19

20 4. Switching controller mode:

21 On switch-on of transistor 27 the current through the inductor
22 24 continues to increase, so that the current sensing signal
23 CS2, which maps the source-side current of transistor 28 and
24 thereby the current from the inductor 24, also has a
25 continuously increasing voltage. The current sensing signal CS2

1 is monitored against an upper limit value. If the charge
2 current flowing through the controlled link of transistor 27
3 and thereby through the coil 24 reaches the upper limit value,
4 the transistor 27 is then switched off. In addition the on
5 duration of the transistor 27 is compared to a second upper
6 limit value. The charge current through the inductor 24 now
7 flows on through the free-wheeling diode 25, in which case it
8 decreases in doing so. The current sensing signal CS2 is now
9 monitored against a lower limit value of the charge current. If
10 the load current reaches the lower limit value, the transistor
11 27 is switched on again. A triangular load current curve is
12 thus produced in the inductor 24 which oscillates between an
13 upper and a lower current limit value. This thus produces a
14 current flow from the input 22 to the output of the switching
15 controller arrangement 21 which has a triangular current curve.

16

17 5. Transition from switching controller mode to complete
18 switch-on:
19 If the switching controller 21 is operated for a long period in
20 switching controller mode in accordance with Para. 4, then as a
21 result the differential voltage Vdiff at switching controller
22 21 will reduce over time. This means that the charge time of
23 the inductor 24 simultaneously increases. If this charge time
24 reaches or exceeds an upper predetermined limit value, it can
25 be assumed that the voltage difference Vdiff at the switching

1 controller 21 is minimal. The transfer gate 29 arranged in
2 parallel to the switching controller can now be closed without
3 danger and thereby switched on. For these purposes transistor
4 27 of the switching controller 21 is now permanently switched
5 on. Likewise transfer gate 29 is switched on via the signal
6 TGon so that the entire switching device is now switched on.
7 The control unit 36 now switches the "Switch ON" signal from a
8 low logical level to a high logical level In this way the
9 present switched-on switch state of the switching device is now
10 signaled externally.

11

12 Figure 4 shows, with reference to a more detailed circuit
13 diagram, a transfer gate of an inventive switching device
14 equipped with a charge pump and activation circuit.

15

16 The transfer gate 29 in the present exemplary embodiment
17 features precisely three parallel-switched branches, with each
18 branch featuring two power MOSFETs T1 - T6. The transfer gate
19 29 essentially has the circuit structure of the transfer gate
20 described with reference to Figure 2.

21

22 Gate terminals and source terminals of transistors T1 - T6 are
23 coupled to each other via a gate protection circuit 40. The
24 gate protection circuit 40 contains a parallel circuit
25 comprising a capacitor C1, a resistor R1 and also a Zener diode

1 D1. The parallel circuit protects the gate terminals of the
2 transistors T1 - T6 on the one hand against a negative gate
3 potential and on the other hand against an overvoltage which
4 could destroy the gate terminals and thereby render the
5 transistors T1 - T6 incapable of functioning.

6

7 A charge pump 41, a switchable oscillator 42 and a switch-off
8 device 43 are further provided for activation of the transfer
9 gate 29.

10

11 The switchable oscillator 42 contains a logic gate 46 as well
12 as a capacitor C6 and a feedback resistor R6. The logic gate 46
13 exhibits a switching behavior susceptible to hysteresis when an
14 input signal is coupled in to it. Advantageously the logic gate 46
15 is embodied as a Schmitt trigger circuit. The logic gate 46
16 features two input terminals, with a first input terminal being
17 connected to the control connection 45 for coupling in the
18 control signal TGon. The second input terminal is connected via
19 capacitor C6 to a supply terminal 39 for a supply potential,
20 for example the reference ground GND. A feedback resistor R6 is
21 arranged between the second input terminal and the output of
22 the logical gate 46.

23

24 The charge pump 41 is connected downstream from the switchable
25 oscillator 42. The charge pump 41 contains an inverter 47, the

1 resistors R4, R5, the capacitors C2 - C5 and the diodes D2 -
2 D6. The charge pump 41 consists of a discharge path and a
3 charge path. The charge path is arranged between the output of
4 the switchable oscillator 42 and the control terminals of the
5 transistors T1 - T6 of the transfer gate 29. The discharge path
6 is arranged between the source terminals of these transistors
7 T1 - T6 and the output of the switchable oscillator 42. The
8 charge path consists of the inverter 47, the resistor R5 as
9 well as the parallel circuit of the capacitors C3, C5, which
10 are connected in series overall. The discharge path consists of
11 the parallel circuit of the capacitors C2, C4 and the resistor
12 R4, which are connected in series to each other. The diodes D2
13 - D6 are provided for coupling the charge path and discharge
14 path.

15

16 The switch-off device 43 contains an inverter 48, the
17 transistors T7, T8 and the resistors R2, R3. The inverter 48 is
18 connected on the input side to the terminal 45 for the control
19 signal TGon. On the output side the inverter 48 is connected to
20 the control connection of the transistor T8. The transistor T8
21 is connected on the emitter side via the resistor R3 to the
22 supply terminal 39. On the collector side the transistor T8 is
23 connected via the resistor R2 to the gate terminals of the
24 transistors T1 - T6. A potential at the tap 49 between the
25 resistor R2 and the collector of the transistor T8 is used for

1 activation of the transistor T7, of which the controlled link
2 is arranged between the gate terminals and source terminals of
3 the transistors T1 - T6.

4

5 The functioning of the circuit arrangement depicted in Figure 4
6 will be briefly explained below:

7

8 The polarity of the differential voltage $V_{diff} = V2 - V1$
9 falling at transfer gate 29 is undefined. For these reasons two
10 of the power MOSFETs T1 - T6 in each case must be connected in
11 series as regards their controlled links to prevent an
12 activation of the body diode inherently present in the relevant
13 power MOSFETs T1 - T6. To increase the current carrying
14 capacity of the transfer gate 29, a number, in the example
15 shown here, three branches with pairs of transistors T1 - T6
16 are arranged in parallel to one another, with each branch of
17 this parallel circuit then carrying a part of the total
18 current. In this way a transfer gate 29 can be provided in a
19 very simple and cost effective way which is in a position to
20 switch very high currents ranging up to 1 kA. Commercially-
21 available low-cost transistors T1 - T6 (power MOSFETs) can
22 advantageously be used for this purpose, which are designed to
23 be used up to 100 A for example.

24

25 Since both the source terminals and also the gate terminals of

1 these power MOSFETs T1 - T6 are switched in parallel, by
2 applying a sufficiently large positive gate source voltage -
3 typically of around 10 - 15 V - the entire transfer gate 29 can
4 be switched on.

5

6 The logic gate 46 advantageously exhibits a switching behavior
7 which is susceptible to hysteresis at its inputs. If for
8 example there is a control signal TGon at the first input
9 terminal of the logic gate 46 which exhibits a high logical
10 level, an oscillating signal occurs at the output of the logic
11 gate 46 of which the oscillation period is determined by the
12 values of feedback resistor R6 and capacitor C6.

13

14 This oscillating output signal Vos of the switchable oscillator
15 42 drives the inverter 47 such that at the output of the gate
16 46 and at the output of the inverter 47 there are now two
17 square-wave signals Vos, Vos', displaced by 180° phases. These
18 two signals, Vos, Vos' now - decoupled via the two current-
19 limiting resistors R4, R5 - drive the phase-opposed charge pump
20 41. The reason for the phase opposition arises from the use for
21 the diodes D2 - D6.

22

23 Now, with each clock of the oscillator signal Vos, the charge
24 of the supply voltage - which typically amounts to around 5 V -
25 is shifted in the charge capacitor C1 by means of the

1 capacitors C2 - C5 and the diodes D2, D6. This means that a
2 voltage builds up at the charge capacitor C1 arranged between
3 the gate terminals and source terminals of the transistors T1 -
4 T6, through which the transistors T1 - T6 are switched on
5 accordingly.

6

7 The selected implementation of the charge pump 41 allows a
8 direct-current-like decoupling of the input potentials of the
9 charge pump, meaning of the signals V_{os}, V_{os'}, and the output
10 potential of the charge pump, meaning the source potential of
11 the transistors T1 - T6.

12

13 In addition the transistor T8 and thereby the transistor T7 are
14 switched via the control signal T_{Gon} and the inverter 48. If
15 the signal T_{Gon} is at a low potential, the transistor T8 is
16 switched on, whereas it is switched off at a high potential.
17 This means that the transistor T8 remains switched off when the
18 charge pump 41 is activated. If the charge pump 41 is switched
19 off by a change in level of the signal T_{Gon} from a high logical
20 level to a low logical level, the transistor T8 is switched on.
21 Thus the control voltage between the gate terminals and source
22 terminals of the transistors T1 - T6 is short circuited, so
23 that these transistors T1 - T6 are switched off. In this way it
24 is possible for transfer gate 29 to switch off very quickly,
25 meaning that it can move into the non-conducting state.

1

2 Figure 5 shows a detailed circuit diagram of the switching
3 controller of the inventive switching device from Figure 3.

4

5 The switching controller 21 contains, as already mentioned,
6 essentially the two transistors 27, 28 as well as the free-
7 wheeling diodes 25, 26 and the inductor 24 arranged between
8 them. A significant element of the switching controller 21 is
9 its activation.

10

11 The transistor 27 arranged on the input side in the switching
12 controller 21, together with the free-wheeling diode 25 and the
13 inductor 24, form the basic elements of a known downward
14 control. In the case of a signal coupled in on the input side
15 via the input terminal 22 the diode 26 is thus inactive and the
16 transistor 28 is switched on statically. If the transistor 27
17 is now switched on via the input signal V_1 the current I_1
18 through the inductor 24 increases constantly, driven by the
19 voltage difference $V_{diff} = V_2 - V_1$ between input 22 and output
20 23. If this current I_1 reaches a predetermined upper limit
21 value, the transistor 27 then switches off and the current I_1
22 through the inductor 24 now flows on through the free-wheeling
23 diode 25. This causes current I_1 to fall until a lower
24 threshold value is reached. At this point transistor 27
25 switches on again and the process starts anew. As a result a

1 current flow I_1 from input 22 to output 23 is produced.

2

3 The current I_1 which flows through the inductor 24, only flows
4 through the transistor 27 as well during the charging-up phase.

5 In the discharging phase the current I_1 does not flow via the
6 transistor 27, but instead via the free-wheeling diode 25. The
7 current I_1 flows simultaneously in both phases, i.e. in the
8 charging phase and also in the discharging phase, through the
9 inversely operated, statically switched-on transistor 28.

10

11 In the present exemplary embodiment the transistors 27, 28 are
12 embodied as power MOSFETs, especially as N-channel power
13 MOSFETs. Such power MOSFETs typically consist of a plurality of
14 transistor cells. In this case each of the transistor cells
15 contains an individual transistor, with the current carrying
16 load paths of the different individual transistors being
17 connected in parallel to each other. The parallel connection of
18 these individual transistors thus produces a significantly
19 higher current carrying capacity in accordance with the number
20 of transistor cells.

21

22 The transistors 27, 28 are preferably embodied as sense-MOSFETs
23 27, 28 in this case. Figure 6 shows the terminal assignment of
24 transistors 27, 28 embodied as such a sense MOSFET, in which
25 case the terminal assignment should correspond to that shown in

1 Figure 5.

2

3 Such a sense MOSFET 27, in addition to its usual function, also
4 offers the option of measuring a current via its controlled
5 link. A sense MOSFET 27 - like a conventional MOSFET - features
6 a gate terminal G for control of the current flow as well as a
7 source terminal S and a drain terminal D, via which the
8 controlled current flows. In addition, with a sense-MOSFET a
9 smaller proportion of the transistor cells are equipped with
10 their own CS (CS = Current Sense) terminal, so that a lower
11 proportion of the source-side load current I_1 can be tapped
12 off. A potential at terminal KS (KS = Kelvin Source) forms the
13 reference of the current sensing. It is thus possible, via
14 terminal KS, to a certain extent in the style of a four-wire
15 measurement, to avoid an error entry through a voltage drop
16 which occurs in the resistance of the bond wire at the terminal
17 S1. To implement a measurement accuracy which is as high as
18 possible the voltage difference between the terminals CS and KS
19 must however be as small as possible, ideally very much smaller
20 than 100 mV. This requires an input impedance of the current
21 sensing circuit which is as small as possible, which is also
22 guaranteed with a sense MOSFET in accordance with Figure 6.

23

24 The particular advantage in using a sense MOSFET according to
25 Figure 6 - as opposed to a measurement of the voltage drop at a

1 measurement resistor (shunt resistor) - lies in the
2 significantly lower power dissipation, since only a very small
3 part of the source current is included for forming the measured
4 values. A sense MOSFET typically has a few 10,000 - 100,000
5 transistor cells. For a sufficiently representative current
6 measurement it is fully sufficient here just to include a few
7 of these transistor cells for the current sensing.

8

9 Current sensing devices 35, 36 are provided in each case for
10 current sensing at transistors 27, 28. The current sensing
11 device 35 contains two measurement paths, which are connected
12 on one side to a supply terminal 39 with the reference
13 potential and on the other side are connected to the
14 measurement terminals KS11, CS11 of the sense MOSFET 27. The
15 first current sensing path consists of the resistor R11 as well
16 as the controlled paths of the transistors T51, T31, which are
17 connected to each other in series and are arranged between the
18 supply connection 39 and terminal KS11. The second current
19 sensing path consists of the resistor R21 as well as the
20 controlled paths of the transistors T61, T41, which are
21 arranged in series between the supply connection 39 and
22 terminal CS11. The transistors T51, T61 as well as the
23 transistors T31, T41 are each arranged in a current balancing
24 circuit, with the transistors T51 and T41 forming the
25 transistor diode of the relevant current balancing element T51,

1 T61;T31, T41 in each case. A tap between the resistor R21 and
2 the transistor T61 forms the output terminal 50, at which the
3 current sensing signal CS1 can be tapped.

4

5 The measurement of a load current flowing through transistor 27
6 is undertaken on the basis of a reference potential KS11, which
7 - depending on the level of the external potentials V1, V2
8 applied at the terminals 22, 23 - varies between a minimum
9 value and around 60 V. For improved further processing in the
10 control unit 30 a potential shift of the current sensing signal
11 CS1 is now undertaken. This can be implemented in an especially
12 elegant way by using the current balancing circuits arranged in
13 each current sensing device 35. In this case the input
14 impedance of the current sensing circuits 35 or of the current
15 balancing circuits must be as low as possible, in order to tap
16 a suitable current sensing signal from the sense MOSFET 27. The
17 current sensed can then be converted into a potential CS1
18 suitable for further processing by means of the resistor R21
19 which can be tapped at output 50 as a current sensing signal
20 CS1.

21

22 The current sensing device 36 has an equivalent structure to
23 the current sensing device 35. However it should be noted here
24 that the transistor 28 will be operated inversely and therefore
25 the terminals of the current measurement circuit at transistor

1 28 are reversed compared to normal operation.

2

3 Figure 7 shows the circuit diagram of an auxiliary power source
4 for supplying the gate control device from Figure 3,

5

6 The auxiliary power source 32 features a transistor T12, the
7 inductor L12 and the double diode D12 which in the circuit from
8 Figure 7 form the basic components of a downward controller.

9

10 If transistor T12 is switched on, as a result of a high
11 potential at the emitter of the transistor T42, an increasing
12 current flows through the inductor L12. This current I_{12} flows
13 at the same time through the current sensing resistor R12. The
14 voltage produced from this is directed via resistor R32 to the
15 base of transistor T22. The connection of a PNP bipolar
16 transistor T22 with an NPN bipolar transistor T32 largely
17 compensates for the influence of the base emitter diode of
18 transistor T32, so that overall a transistor with a very low
19 base emitter voltage difference is produced. These transistors
20 T22, T32 connected cascaded thus to a certain extent form a
21 "supertransistor".

22

23 The emitter potential of the transistor T32 is set by the
24 voltage divider, consisting of the resistors R52, R62, to an
25 upper threshold value. If the current I_{12} through transistor

1 T12 is close to zero, the base potential of the
2 "supertransistor" T22, T32 is also zero and the transistor T12
3 blocks. The collector potential of this "supertransistor" T32,
4 T22 is raised to around 5 V via the resistor R42, with the
5 result that the basic voltage of the transistor T42 connected
6 to it also increases. The emitter voltage of the transistor T42
7 thus also increases to around 4.3 V. This transistor T42 is
8 coupled on the emitter side to the control connection of
9 transistor T12. The given voltage value of 4.3 V is sufficient
10 to switch on the T12. With increasing current I12 through the
11 elements L12, T12, R12 the voltage falling via the resistor R12
12 thus increases and thereby also the voltage falling via the
13 resistor R32 for activation of the base of the
14 "supertransistor" T22, T32. If a value is now reached which
15 corresponds to the upper threshold value set at the emitter of
16 transistor T32, transistor T32 switches on, at which point its
17 collector potential drops. As a result of this the emitter
18 voltage of transistor T42 drops and with it the gate voltage of
19 transistor T12. Transistor T12 then switches off. Driven by the
20 induction voltage over the coil L12 functioning as a choke, the
21 voltage at the drain terminal of the transistor T12 will now
22 rise until the double diode D1 begins to conduct current. The
23 energy stored in the inductor L12 is now discharged via the
24 capacitor C12 or respectively on reaching the breakdown voltage
25 of the Zener diode D22 via this diode D22.

1
2 At the same time the potential at the center tap 70 of the
3 double diode D12 increases via the potential V1 present at
4 input 22, at which point transistor T52 becomes conductive and
5 current I22 limited by the resistor R82 flows over the
6 controlled link of transistor T52. This current I22 creates a
7 voltage increase at resistor R32 which switches on transistors
8 T22, T32. This keeps the base potential of transistor T42 at a
9 low value and as a result of this transistor T12 remains
10 switched off.

11
12 If inductor L12 is now completely discharged, the voltage over
13 the inductor L12 collapses. Transistor 52 likewise blocks and
14 the voltage at resistor R32 drops towards zero. This means that
15 the "supertransistor" T22, T32 again switches off, at which
16 point its collector potential rises. The emitter voltage of the
17 transistor T42 now also increases and transistor T12 will be
18 switched on again. This creates a triangular current in the
19 inductor L12 which oscillates backwards and forwards between
20 the upper threshold value and zero. In the charge phase the
21 inductor L12 takes charge from the potential V1 present at
22 input 22 and in the discharge phase this charge is passed on to
23 the storage capacitor C12. The potential Vaux1 thus produced
24 can be tapped at the output 71 and supplies the gate control
25 device 31 of a power MOSFET in case, in the present example the

1 power MOSFET 27.

2

3 Figure 8 shows a circuit diagram of a gate-control device 30
4 for controlling the switching controller from Figure 3.

5

6 The gate control device 30 can be supplied with a supply
7 potential V_{aux1} which can be decoupled at the supply terminal
8 71 created by the auxiliary voltage source 32. The gate control
9 device 30 further features another control connection 72 which
10 is coupled to the control device 36 and via which a control
11 signal $Ctrl1$ can be decoupled. Using the level of this signal
12 $Ctrl1$ the control unit 36 of the gate control device 30
13 determines the switching status of the power MOSFET 27. If the
14 control signal $Ctrl1$ has a low logical level (LOW) transistor
15 T13 is switched to zero current. The transistor T23 is then
16 also switched off, since its base emitter voltage is zero in
17 this case. The resistor R63 defines the base potential of the
18 transistor T33 on the source voltage of the power MOSFET 27, at
19 which point the transistor T33 switches and the potential at
20 terminal 74 largely approaches the value of the potential at
21 terminal 73. The terminal 73 is connected to the source
22 terminal S11, the terminal 74 is connected to the gate terminal
23 G11 of the power MOSFET 27. As a result the gate source voltage
24 of the power MOSFET 27 is approximately zero so that this
25 MOSFET 27 is switched off.

1 If the control signal Ctrl1 at the control input 72, controlled
2 by the control unit 36, jumps to a high logical level (HIGH),
3 transistor T13 becomes conductive. Transistor T13 operates in
4 connector with resistor R23 as a current source, for which the
5 value is essentially determined by the level of the control
6 signal Ctrl1 and the value of the resistor R23. The load
7 current through this transistor T13 is used for base activation
8 of the transistor T23, which is configured by means of the
9 resistors R43, R53 and the diode D13 as current balancing
10 element. The current flow through transistor T23 now charges
11 the gate capacitor of the power MOSFET 27 via terminal 74. This
12 means that the gate source voltage (voltage between the
13 terminals 73, 74) of the power MOSFET 27 and the power MOSFET
14 27 is finally switched on.

15
16 If the control signal Ctrl1 jumps to a low logical level,
17 transistor T13 switches off, at which point the transistor T23
18 is also switched to no-load. Transistor T33 is now switched to
19 conducting via resistor R63, at which point the gate source
20 voltage of the MOS transistor 27 is controlled via the
21 transistor T33 and the resistor R73 is controlled to
22 approximately 0 V. Transistor T27 then switches off.

23
24 In the same way the power MOSFET 28 is switched on via an
25 equivalently embodied gate control device 32 or is switched

1 off.

2

3 Figure 9 shows a circuit diagram of the voltage sensing device
4 37 from Figure 3.

5

6 The voltage sensing device 37 essentially consists of a first
7 differential amplifier 80, a voltage comparator 81, a two-pole
8 switch S1a, S1b and a second differential amplifier 82.

9

10 The first differential amplifier 80 is connected on the input
11 side via the resistor R110, R130 to the terminals 22, 23. The
12 first differential amplifier 80 thus converts the differential
13 voltage $V_{diff} = V_2 - V_1$ present between the terminals 22, 23 to
14 a voltage related to a reference voltage V_{ref} . For the case in
15 which the first differential amplifier 80 is supplied with a
16 supply voltage of 5 V, a reference voltage $V_{ref} = 2.5$ V is
17 advantageous, since the measured differential voltage V_{diff} can
18 features both a positive and also a negative polarity. Let a
19 positive polarity of the differential voltage V_{diff} be given
20 below.

21

22 The voltage difference V_{diff} between the terminals 22, 23 is
23 recorded in the differential amplifier consisting of the
24 resistors R110, R120, R130, R140 and the first differential
25 amplifier 80 and is converted into a DC voltage related to a

1 predetermined reference voltage V_{ref} . If the potential
2 difference amounts to 0 V, a voltage V_{ref} can be tapped off at
3 the output of the differential amplifier 80.

4

5 It should further be noted that the input potentials V_1 , V_2 can
6 under some circumstances have high values in the range of
7 around 60 V, but the differential voltage $V_{diff} = V_2 - V_1$ with
8 increasing charge equalization becomes relatively small, for
9 example is in the range of less than 1 V. For these reasons the
10 first differential amplifier 80 must feature the best possible
11 common-mode rejection.

12

13 A voltage comparator 81 connected downstream from the first
14 differential amplifier 80 now compares the output voltage of
15 the first differential amplifier 80 with the reference
16 potential V_{ref} . Regardless of whether this output voltage is
17 greater than or less than the reference voltage V_{ref} , the
18 voltage comparator 81 activates one of the two controllable
19 switches S_{1a} , S_{1b} on the output side. The controllable switches
20 S_{1a} , S_{1b} are coupled to each other and can for example be
21 embodied as a CMOS changeover switch.

22

23 This controlled switchover of the switches S_{1a} , S_{1b} coupled to
24 each other always activates a downstream, second differential
25 amplifier 82 with a signal of the same polarity. In the present

1 exemplary embodiment the second differential amplifier 82 is
2 always activated with a positive input voltage. The second
3 differential amplifier 82 is connected in a circuit with the
4 resistors R150, R160, R170, R180. Since the reference potential
5 GND of the second differential amplifier 82 is a ground
6 potential GND (not shown in Figure 9), the second differential
7 amplifier 82 thus creates the absolute value of the
8 differential voltage Vdiff coupled-in on the input side in the
9 voltage sensing device 37 related to the reference ground. This
10 signal Vdiff2 present on the output side at the second
11 differential amplifier 82 can be tapped off at the output
12 terminal 83 and can thus be fed to the control unit 36. The
13 signal Vdiff2 thus forms a voltage sensing signal which
14 specifies the absolute value or the amount of the differential
15 voltage Vdiff.

16

17 The output signal of the comparator 81 equally forms the signal
18 Vdiff1, which can be tapped off at the output terminal 84 and
19 is directed to the control unit 36 of the differential voltage
20 Vdiff. The signal Vdiff1 thus forms a voltage sensing signal,
21 which specifies the polarity or the leading sign of the
22 differential voltage Vdiff.

23

24 Figure 10 shows, with reference to a block diagram, the
25 structure of the control unit 36 for an inventive switching

1 device.

2 The control unit 36 consists of two comparators 90, 91, a
3 switchover unit 92, two further comparators 93, 94, a PWM
4 generator 95 with time monitoring, a logic unit 96 and a
5 diagnosis unit 97.

6

7 The comparators 90, 91 compare the absolute value of the
8 differential voltage V_{diff2} with an upper voltage value V_{o1} and
9 a lower voltage value V_{u1} and from this creates the two logic
10 signals V_{o2} , V_{u2} , which will be routed to the logic unit 96. If
11 the potential V_{diff2} is greater than V_{o1} , the output signal V_{o2}
12 of the comparator 90 has a high logical level. If the value of
13 the potential V_{diff2} is smaller than V_{u1} , the output signal V_{u2}
14 has a low logical level.

15

16 The current sensing signals CS1, CS2 of the current sensing
17 devices are routed to the switchover unit 92. The switchover
18 unit 92 is further activated via a control signal SEL of the
19 logic unit 96. Controlled by this control signal SEL the
20 switchover unit 92 directs the current sensing signal CS1 or
21 the current sensing signal CS2 to the downstream comparators
22 93, 94.

23

24 These comparators 93, 94 are embodied as current comparators.
25 The comparator 93 compares the signal coupled in on the input

1 side (CS1 or CS2) with an upper current value and on the output
2 side creates the current signal I_{max} . The comparator 94
3 compares the signal (CS1 or CS2) coupled in on the input side
4 with a lower current value I and creates the current signal
5 I_{min} . If the current sensing signal CS1 or CS2 is greater than
6 I_o , the current signal I_{max} has a high logical level. If the
7 current sensing signal CS1 or CS2 is less than I , the current
8 signal I_{min} has a low logical level. The signals I_{max} , I_{min} are
9 coupled into a PWM generator 95 connected downstream from the
10 comparators 93, 94.

11

12 The PWM generator 95 creates at its PWM output a pulse-value
13 modulated signal PWM_{out} depending on the signal level of the
14 signals I_{max} , I_{min} . If the signal I_{max} has a high logical
15 level, a signal PWM_{out} with a low logical level is present at
16 the PWM output of the PWM generator 95. This is the signal to
17 indicate that the upper current value I_o was exceeded and that
18 the transistor 27, 28 selected for PWM operation must be
19 switched off. The signal level PWM_{out} at the PWM-output of the
20 PWM generator 95 is retained until such time as the level of
21 the signals I_{min} jumps from a high logical level to a low
22 logical level. This signal changeover is the indication that
23 the lower current value I was undershot and that the
24 transistors 27, 28 selected for PWM operation must be switched
25 on. With the change of level of the signal I_{min} from the low

1 logical level LOW to the high logical level HIGH the signal
2 PWMout at the PWM output of the PWM generator 95 thus jumps
3 back to a high logical level.

4

5 In one embodiment the PWM generator 95 further features a
6 monitoring circuit which compares the on duration of the signal
7 at the PWM output PWMout with an upper limit value and if this
8 limit value is exceeded, creates a "Timeout" signal at the
9 timeout output of the PWM generator 95. This "Timeout" signal
10 is coupled into a corresponding timeout input of the logic unit
11 96.

12

13 The logic unit 96 controls the further functional sequence of
14 the control unit 36 with reference to the described signals as
15 well as on the basis of the external "On/Off" signal. The logic
16 unit 96 detects on the basis of the size and the leading sign
17 of the differential voltage Vdiff whether the power switch 27,
18 28 must be operated in switching controller mode. Furthermore
19 the logic unit 96 decides which of the two power transistors
20 27, 28 are to be activated as switching control transistors and
21 which are to be switched on completely.

22

23 In the present exemplary embodiments it has been assumed in
24 each case that the power transistor 27 will be operated as a
25 switching control transistor and the power transistor 28 then

1 functions as a statically switched-on transistor. If the
2 voltage difference $V1-V2$ is negative, the operation of these
3 two transistors 27, 28 is reversed.

4

5 The logic unit 96 decides which of the two current sensing
6 signals CS1, CS2 is to be used and activates the changeover
7 switch 92 accordingly. The logic unit 96 forwards the pulse
8 width modulated output signal PWMout which can be tapped off at
9 the PWM output of the PWM generator 95 via the control outputs
10 Ctrl11, Ctrl12 to the relevant power transistors 27, 28 selected
11 as switching control transistors.

12

13 The logic unit 26 further detects on the basis of the signals
14 $Vu2$ or "Time out" respectively when the differential voltage
15 $Vdiff$ is small enough or when the charge equalization is far
16 enough advanced to allow the switching controller 21 to be
17 closed without any danger and thereby to switch on the transfer
18 gate 29. Subsequently the logic unit 96 signals to an external
19 control unit not shown in the Figures of the drawing the new
20 switching state by changing the level of the output signal
21 "Switch ON".

22

23 Figure 10 further shows, as a component of the control unit 36,
24 a diagnosis device 97, for which no further details are
25 provided however, since known methods of operation can be used

1 here. Essentially the diagnosis unit monitors 97 a correct
2 function of the circuit parts and circuit elements described
3 above as well as the correct functional sequence overall. The
4 diagnosis unit 97 can also - such as in the event of an
5 external error, such as a short circuit at one of the inputs
6 22, 23 - prevent the inventive switching device 20 or the power
7 MOSFETs 27, 28 being switched on. The output signal DG1 present
8 at the output of the diagnosis device signals to an external
9 control unit whether the switching device 20 or the power
10 MOSFETs 27, 28 operated in switching controller mode are
11 functioning correctly. In an expanded embodiment with a
12 bidirectional data bus not shown the communication of detailed
13 information about the inventive switching device 20 is possible
14 in the event of an error in order to simply a repair to this
15 circuit in this way.

16

17 Although the present invention has been described above on the
18 basis of a concrete preferred exemplary embodiment in great
19 detail, it can be changed and modified in a wide variety of
20 ways.

21

22 Thus the invention is not restricted to the concrete circuit
23 implementations described above. Instead the transfer gate, the
24 switching controller, the control unit, the gate controllers,
25 the current sensing devices, the voltage sensing device, etc.

1 can obviously be embodied in a plurality of different circuit
2 variants, without deviating from the basic principle of the
3 present invention.

4

5 The object of the invention is the provision of a power switch
6 which features a transfer gate expanded by a switching
7 controller. A conventional downward controller can be used here
8 as a switching controller, as has been explained above. Other
9 types of controller, such as an upward controller for example,
10 would also be conceivable in addition or as an alternative.

11

12 Thus the invention is also not just restricted to the actual
13 components used. Instead for example by swapping the
14 conductivity types N for P and vice-versa many other switching
15 examples can be specified. Here too the transistors do not
16 necessarily have to be embodied as bipolar transistors or MOS
17 transistors, but any other transistor types, for example JFETs,
18 thyristors, IGBTs or such like can be used can be connected to
19 one another. It is taken as read that the resistors,
20 capacitors, coils, diodes can be replaced by any resistive
21 elements, capacitive elements inductive elements or rectifying
22 elements. In addition the transistors can be replaced by any
23 controlled switch or amplifying elements depending on the
24 operating modes in which these are to be operated.

25

1 Nor is the invention restricted to specific values. Such
2 figures have merely been given to aid understanding, but should
3 not however restrict the invention in any way.